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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/674,984	01/08/2001	Volker Becker	10191/1565	9242
26646	7590	11/12/2003	EXAMINER	
KENYON & KENYON ONE BROADWAY NEW YORK, NY 10004			COLEMAN, WILLIAM D	
			ART UNIT	PAPER NUMBER
			2823	

DATE MAILED: 11/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/674,984	BECKER ET AL.
	Examiner W. David Coleman	Art Unit 2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 08 September 2003.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 23-48 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 23-48 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. _____.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.

4) Interview Summary (PTO-413) Paper No(s) _____.

5) Notice of Informal Patent Application (PTO-152)

6) Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed September 8, 2003 have been fully considered but they are not persuasive.
2. Applicants contend that the rejection under 35 U.S.C. § 103(a) as being unpatentable over Yakura in view of Blayo should be withdrawn.
3. Applicants contend that Yakura purportedly concerns a method and structure for sensing temperature data of a batch group of silicon wafers and that a physical measured quantity that is proportional to the extend of an at least locally etched lateral undercut of a structured surface layer of a sacrificial layer.
4. In response to Applicants contention that the combined teachings fail to teach the claimed invention, please note that independent claims 23 and 31 does not preclude the measurement of temperature as described by Yakura.
5. Applicants contend that Yakura does not disclose at least one passive electronic component arranged on a structured surface layer of a sacrificial layer and in the shape of a coil for determining a physical quantity that is proportional to the extend of an at least locally etched lateral undercut of the structured surface layer as recited in claim 23.
6. In response to Applicants contention that the combined teachings fail to teach at least one passive electronic component arranged on a structured surface layer of a sacrificial layer and in the shape of a coil for determining a physical quantity that is proportional to the extend of an at least locally etched lateral undercut of the structured surface layer as recited in claim 23.

Applicants are directed to the combined references. By the reviewing of Applicants claims,

Applicants cannot provide any reasonable proof that the claimed “sacrificial layer” remains or is removed, nor does Applicants disclose any particular location of the so-called sacrificial layer, since these are product claims. First, Yakura teaches a passive component (i.e., coil which measures a physical quantity as claimed). Second, since Yakura discloses an RC circuit as seen in FIG. 1, Yakura discloses a well known circuit which has a predetermined frequency due to the resistive elements 20 and capacitive elements 18 in the circuit), it is well known in the art that RC circuits produce frequencies determined by the values of the resistance and capacitance given. Thirdly, Applicants are claiming an invention with intended use limitations in product claims. The terms “locally etched lateral undercut” are process limitations as well as the term “sacrificial layer”. There is no way to enforce the claimed invention since the invention is directed to product claims with process limitations and intended use features. Applicants are directed to Corning Glass Works, 868 F.2d at 1257, 9 USPQ2d at 1966. Please note that Blayo has support for the prior art rejection because Blayo discloses a device that measures a physical quantity as claimed, which also includes an etched lateral undercut. Because Applicants broadly and vaguely claims a monitoring device and fails to teach or disclose a specific device, Blayo meets the teaching or motivation of the claimed invention.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 23-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yakura et al., U.S. Patent 5,576,224 in view of Blayo et al., U.S. Patent 5,739,909.

8. Pertaining to claim 23, Yakura discloses a semiconductor device substantially as claimed. See **FIGS. 1 - 5**, where Yakura teaches a device for determining an extent of an at least locally undercut of a structured surface layer on a sacrificial layer, comprising:

at least one passive electronic component **44** arranged on a the structured surface layer for determining a physical measured quantity. However, Yakura fails to disclose that the coil is proportional to the extent of the lateral undercut. Blayo teaches an etched lateral undercut. In view of Blayo, it would have been obvious to one of ordinary skill in the art to incorporate the etched lateral undercut of Blayo in the Yakura semiconductor device because processing methods to generate sub-micron features typically employ plasma etching (column 1, lines 24-25).

9. Pertaining to claim 24, Blayo teaches wherein the physical measured quantity corresponds to one of:

a capacitance,
one of an absorbed intensity and an emitted intensity of an electromagnetic emission,
one of an absorbed frequency and an emitted frequency, and
one of an absorbed frequency spectrum and an emitted frequency spectrum of the electromagnetic emission.

10. Pertaining to claim 25, Blayo teaches wherein the one of the absorbed frequency and the emitted frequency corresponds to a resonance frequency.
11. Pertaining to claim 26, Blayo teaches wherein at least one transmitter **20** for emitting a first signal;
at least one receiver **60** for detecting a second signal, the at least one passive electronic component **40** interacting with the first signal and one of generating the second signal and transforming the first signal into the second signal.
12. Pertaining to claim 27, Blayo teaches wherein the physical measured quantity is determined from one of:
the second signal, and
a difference between the first signal and the second signal and the second signal.
13. Pertaining to claim 28, Blayo, teaches wherein the at least one transmitter and the at least one receiver are integrated in an assembly.
14. Pertaining to claim 29, Blayo teaches wherein the assembly includes a processing unit.
15. Pertaining to claim 30, Blayo teaches wherein the at least one transmitter is at the same time also the at least one receiver.
16. Pertaining to claim 37, Blayo teaches wherein the structured surface layer, at least in an area of the at least one passive electronic component, is separated from a base layer by the sacrificial layer.
17. Blayo discloses a semiconductor device substantially as claimed as discussed above, however, Blayo fails to teach the following limitations.

Pertaining to claims 33, 35 and 37, Blayo fails to teach wherein the coil delineated out in the structure surface layer and including a first coil end and a second coil end, the coil and a base layer arranged with respect to the structured surface layer and the sacrificial layer form a capacitor having a capacitance proportional to the extent of the lateral undercut. Yakura teaches a passive electron component which includes a coil delineated out in the structure surface layer and including a first coil end and a second coil end, the coil and a base layer arranged with respect to the structured surface layer and the sacrificial layer form a capacitor having a capacitance proportional to the extent of the lateral undercut. See **FIG 4.**, where Yakura teaches an inductor having a built in capacitor (parasitic capacitor). In view of Yakura, it would have been obvious to one of ordinary skill in the art to incorporate the passive component of Yakura into the Blayo semiconductor device because processing methods to generate sub-micron features typically employ plasma etching (column 1, lines 24-25).

18. Pertaining to claims 36, Blayo fails to teach wherein at least one of the first coil end is dimensioned in an extent thereof such that a complete undercut of the at least one of the first coil end and the second coil end does not occur. Yakura teaches wherein at least one of the first coil end is dimensioned in an extent thereof such that a complete undercut of the at least one of the first coil end and the second coil end does not occur. See **FIG. 4** of Yakura where the coil ends are not undercut. In view of Yakura, it would have been obvious to one of ordinary skill in the art to not undercut the coil ends in the Blayo semiconductor device because the motivation is to provide a stable platform for the coil ends.

19. Claims 38, 39, 40, 41 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blayo et al., U.S. Patent 5,739,909 in view of Yakura et al., U.S. Patent 5,539,241 as applied to claims 23-30, 33, 35, 36 and 37 above, and further in view of Curran, U.S. Patent 5,126,284.

20. Pertaining to claims 38 and 39, the combined teachings of Blayo and Yakura fail to disclose a semiconductor device wherein a structure of the base layer corresponds to one of: a material including silicon and polysilicon, and a silicon wafer. Curran teaches providing a material of silicon and a silicon wafer. See **FIG. 1** of Curran, wherein an inductor composed of silicon and a silicon wafer is disclosed. In view of Curran, it would have been obvious to one of ordinary skill in the art to incorporate silicon into the combined teachings of Blayo and Yakura because silicon is highly useful in silicon-based solid-state electronic devices (column 7, lines 36-37).

21. Pertaining to claims 40, 41 and 42 the combined teachings of Blayo and Yakura fail to teach a silicon oxide layer and a structured surface layer including trenches that extend in depth down to the sacrificial layer wherein the trenches border a structure to be under cut, in the structured surface area. Curran teaches a silicon oxide layer and a structured surface layer including trenches that extend in depth down to the sacrificial layer wherein the trenches border a structure to be under cut. In view of Curran, it would have been obvious to one of ordinary skill in the art to teach a silicon oxide layer and a structured surface layer including trenches that extend in depth down to the sacrificial layer wherein the trenches border a structure to be under cut in the combined teachings of Blayo and Yakura because the motivation would be to make passive electronic devices that are three dimensional and functional.

Conclusion

22. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

23. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

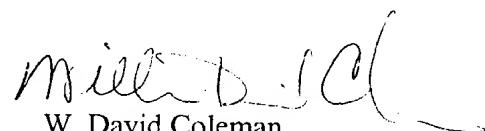
24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 703-305-0004. The examiner can normally be reached on 9:00 AM-5:00 PM.

25. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

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26. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.


W. David Coleman
Primary Examiner
Art Unit 2823

WDC